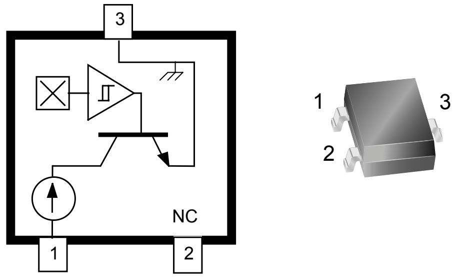
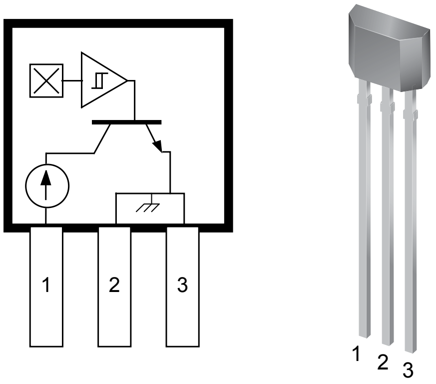
A1242

Two-Wire Chopper-Stabilized Hall Effect Latch

Package LH, 3-pin Surface Mount



Package UA, 3-pin SIP



ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	**28 V**
Reverse-Supply Voltage, V_{RCC}	**–18 V**
Magnetic Flux Density, B	**Unlimited**
Operating Temperature	
Ambient, T_A, Range E	**–40ºC to 85ºC**
Ambient, T_A, Range L	**–40ºC to 150ºC**
Maximum Junction, $T_{J(max)}$	**165ºC**
Storage Temperature, T_S	**–65ºC to 170ºC**

The A1242 Hall effect latch is a two-wire latch especially suited for operation over extended temperature ranges, from –40 to +150°C. Superior high-temperature performance is made possible through the Allegro® patented dynamic offset cancellation technique, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

The current-switching output technique allows for the reduction in cost in the wiring harness because only two connections to the sensor are required. The current-switching output structure also inherently provides more immunity against EMC/ESD transients. These sensors have low magnetic thresholds, thereby enabling more flexibility in the magnetic circuit design.

The Hall effect latch will be in the high output current state in the presence of a magnetic South Pole field of sufficient magnitude and will remain in this state until a sufficient North Pole field is present.

The A1242 includes the following on a single silicon chip: a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a current source output. Advanced BiCMOS wafer fabrication processing takes advantage of low-voltage requirements, component matching, very low input-offset errors and small component geometries.

Suffix 'L-' devices are rated for operation over a temperature range of –40°C to +150°C; suffix 'E-' devices are rated for operation over a temperature range of –40°C to +85°C. Two A1242 package styles provide magnetically optimized solutions for most applications. Package LH is a SOT23W, a miniature low-profile surface-mount package, while package UA is a three-lead ultra-mini SIP for through-hole mounting. Each package is available lead (Pb) free, with 100% matte tin plated leadframes.

Features and Benefits

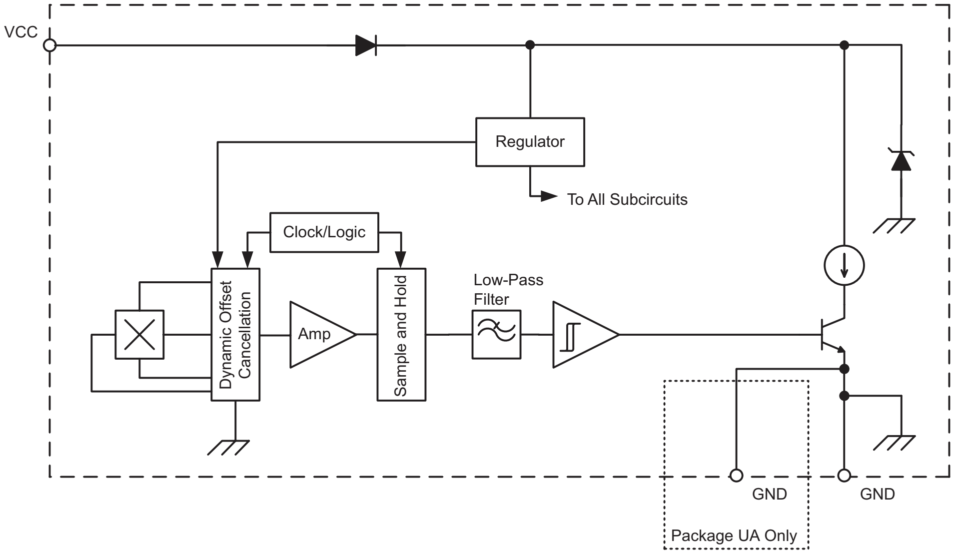
- Chopper stabilization
  - Superior temperature stability
  - Extremely low switchpoint drift
  - Insensitive to physical stress
- Reverse battery protection
- Solid-state reliability
- Small size
- Robust EMC capability
- High ESD ratings (HBM)

Product Selection Guide

Part Number	Packaging*	Mounting	Low Current, $I_{CC(L)}$ (mA)	Ambient, T_A (°C)	$B_{RP(MIN)}$ (G)	$B_{OP(MAX)}$ (G)
A1242ELHLT-I1-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	5.0 to 6.9	–40 to 85	–80	80
A1242ELHLT-I2-T			2.0 to 5.0			
A1242EUA-I1-T	Bulk, 500 pieces/bag	3-pin SIP through hole	5.0 to 6.9			
A1242EUA-I2-T			2.0 to 5.0			
A1242LLHLT-I1-T	7-in. reel, 3000 pieces/reel	3-pin SOT23W surface mount	5.0 to 6.9	–40 to 150		
A1242LLHLT-I2-T			2.0 to 5.0			
A1242LUA-I1-T	Bulk, 500 pieces/bag	3-pin SIP through hole	5.0 to 6.9			
A1242LUA-I2-T			2.0 to 5.0			

*Contact Allegro for additional packing options.

Functional Block Diagram



Terminal List

Name	**Description**	**Number**	
		Package LH	**Package UA**
VCC	Connects power supply to chip	1	1
GND	Ground	3	2,3
NC	No internal connection	2	–

ELECTRICAL CHARACTERISTICS over full operating voltage and temperature ranges, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Electrical Characteristics						
Supply Voltage[2] [3]	V_{CC}	Operating, T_J < 165°C	3.5	–	24	V
Supply Current	$I_{CC(L)}$	-I1, $B < B_{RP}$	5	–	6.9	mA
		-I2, $B < B_{RP}$	2	–	5	mA
	$I_{CC(H)}$	-I1 and -I2, $B > B_{OP}$	12	–	17	mA
Output Slew Rate[4]	dI/dt	R_S = 100 Ω, C_S = 20 pF, no bypass capacitor	–	36	–	mA/µs
Chopping Frequency	f_C		–	200	–	kHz
Power-On Time	t_{PO}	$V_{CC} > V_{CC(MIN)}$	–	–	25	µs
Power-On State[5]	POS	$t_{PO} < t_{PO(max)}$, dV_{CC}/dt > 25 mV/µs	–	$I_{CC(H)}$	–	–
Supply Zener Clamp Voltage	$V_{Z(supply)}$	I_{CC} = 20 mA; T_A = 25°C	28	–	–	V
Supply Zener Current[6]	$I_{Z(supply)}$	V_S = 28 V	–	–	20	mA
Reverse Battery Current	I_{RCC}	V_{RCC} = –18 V	–	–	2.5	mA
Magnetic Characteristics[7]						
Operate Point	B_{OP}	South pole adjacent to branded face of device	5	32	80	G
Release Point	B_{RP}	North pole adjacent to branded face of device	–80	–32	–5	G
Hysteresis	B_{HYS}	$B_{OP} – B_{RP}$	40	64	110	G

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see *Power Derating* section.
[3] V_{CC} represents the generated voltage between the V_{CC} pin and the GND pin.
[4] The value of dI is the difference between 90% of $I_{CC(H)}$ and 10% of $I_{CC(L)}$, and the value of dt is time period between those two points. The value of dI/dt depends on the value of the bypass capacitor, if one is used, with greater capacitances resulting in lower rates of change.
[5] For t > $t_{PO(max)}$, and $B_{RP} < B < B_{OP}$, POS is undefined.
[6] Maximum current limit is equal to the maximum $I_{CCL(max)}$ + 3 mA.
[7] Magnetic flux density, B, is indicated as a negative value for north-polarity magnetic fields, and as a positive value for south-polarity magnetic fields. This so-called algebraic convention supports arithmetic comparison of north and south polarity values, where the relative strength of the field is indicated by the absolute value of B, and the sign indicates the polarity of the field (for example, a –100 G field and a 100 G field have equivalent strength, but opposite polarity).

DEVICE QUALIFICATION PROGRAM

Contact Allegro for information.

EMC (Electromagnetic Compatibility) PERFORMANCE

Contact Allegro for information.

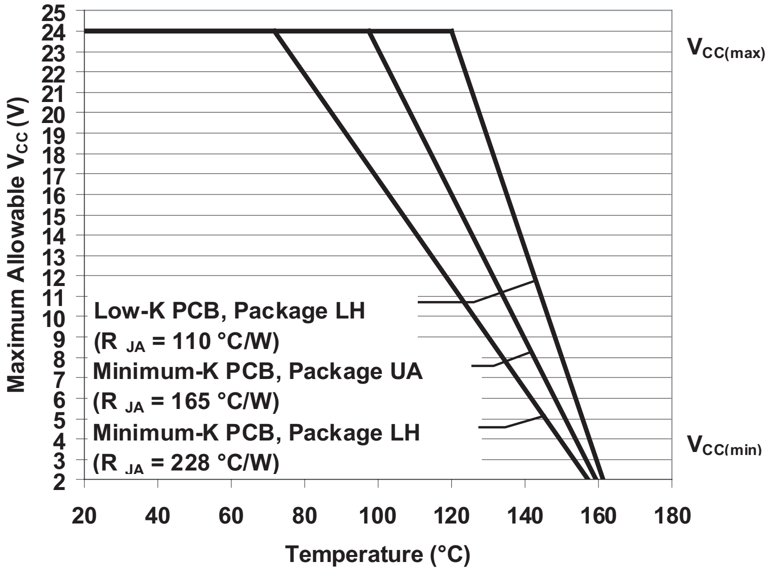
THERMAL CHARACTERISTICS may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package LH, minimum-K PCB (single layer, single-sided with copper limited to solder pads)	228	ºC/W
		Package LH, low-K PCB (single layer, double-sided with 0.926 in^2 copper area)	110	ºC/W
		Package UA, minimum-K PCB (single layer, single-sided with copper limited to solder pads)	165	ºC/W

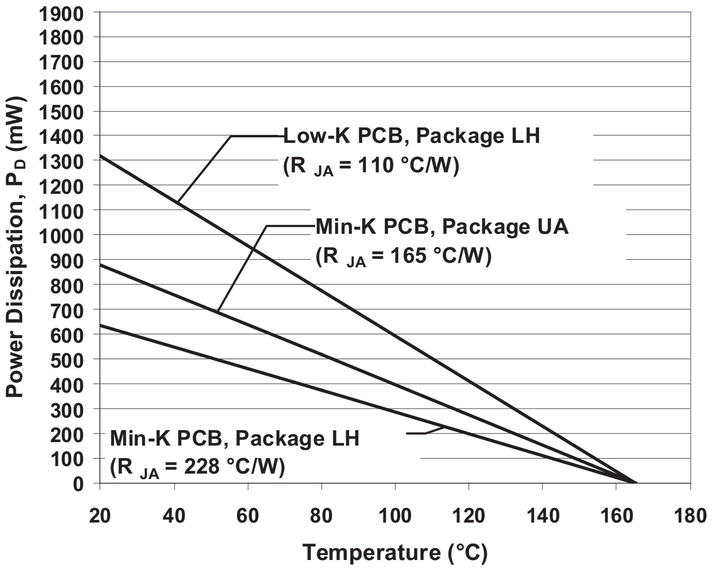
*Additional information available on the Allegro Web site.

Power Derating Curve

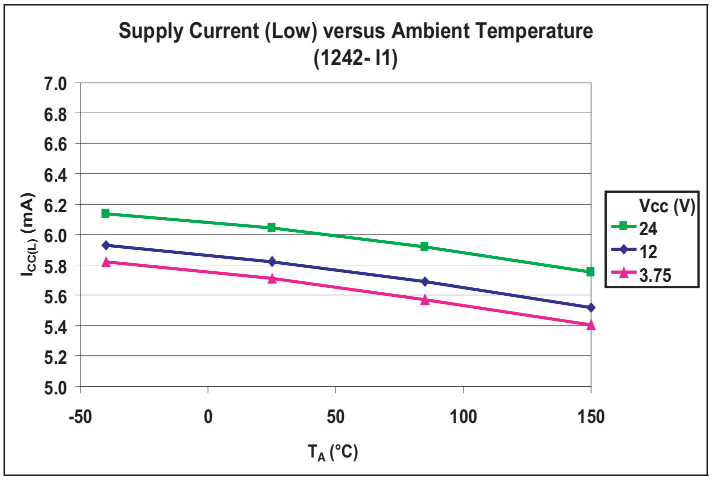
$T_{J(max)}$ = 165°C; I_{CC} = $I_{CC(max)}$

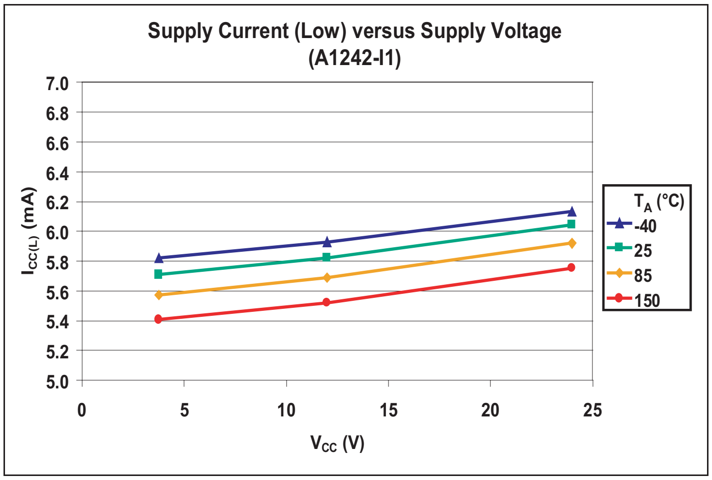


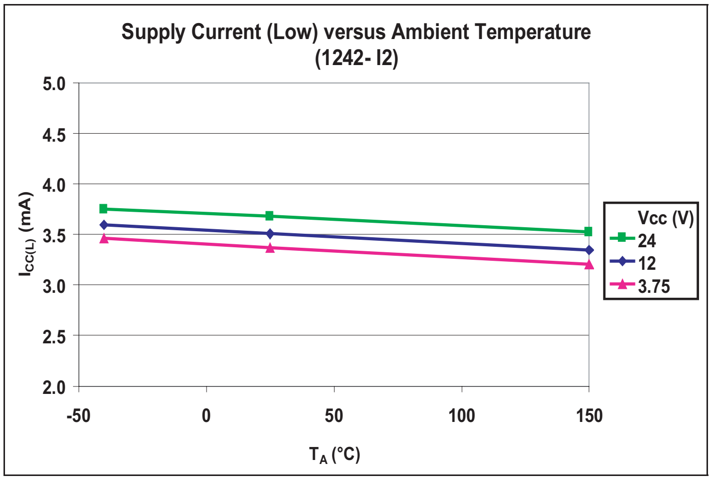
Power Dissipation versus Ambient Temperature

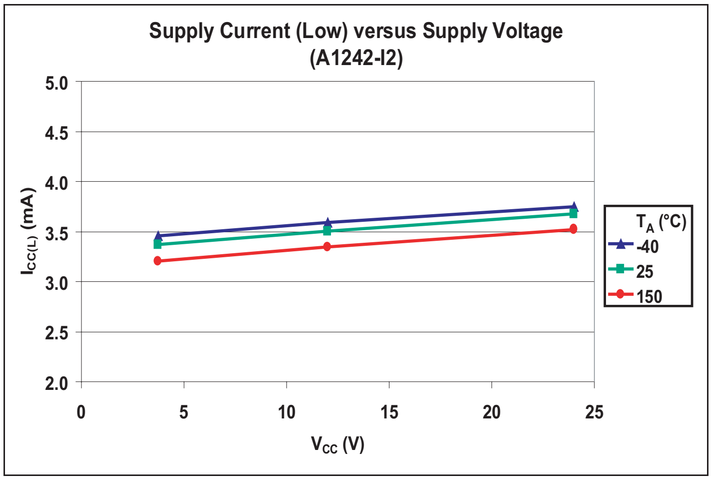


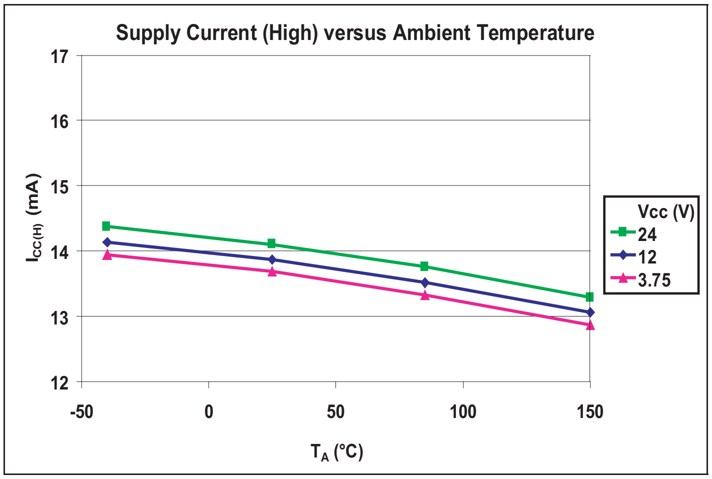
Characteristic Data

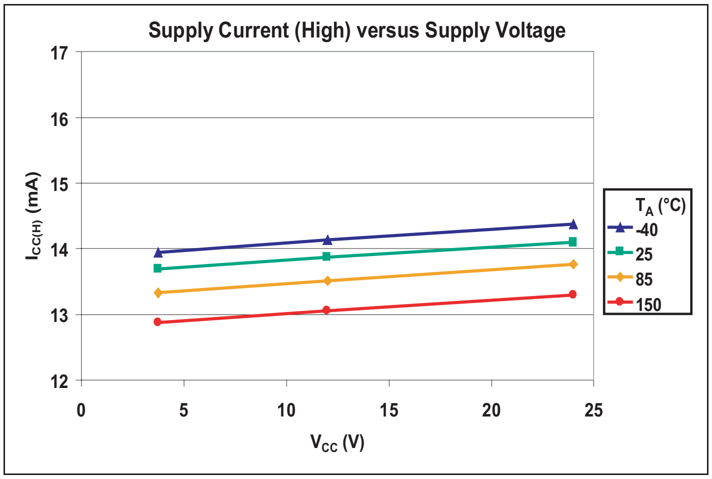


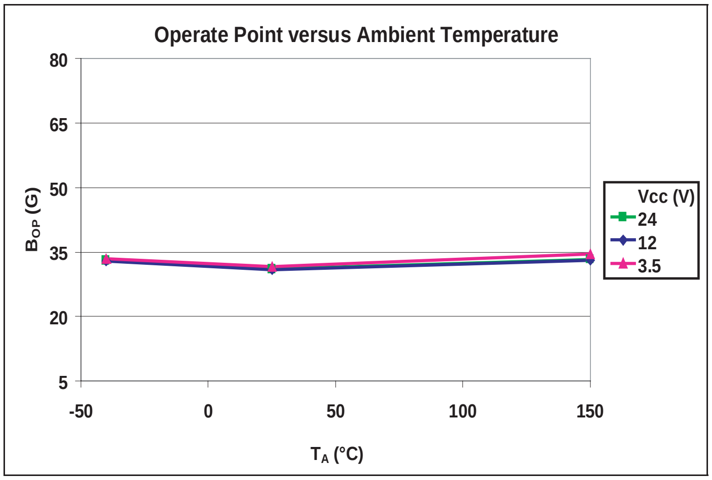


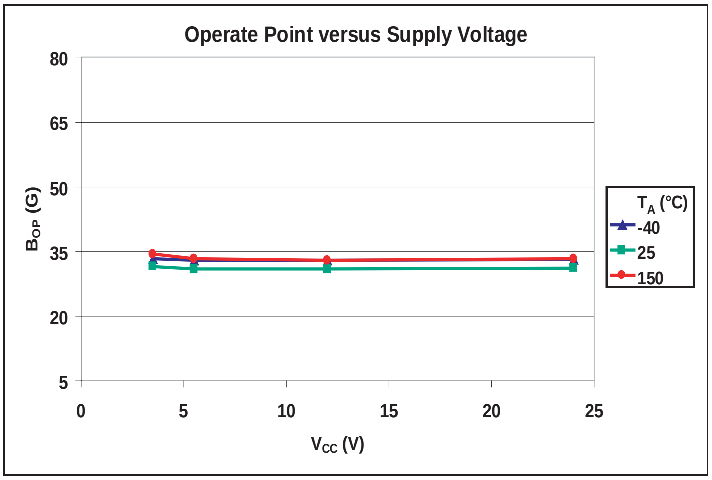


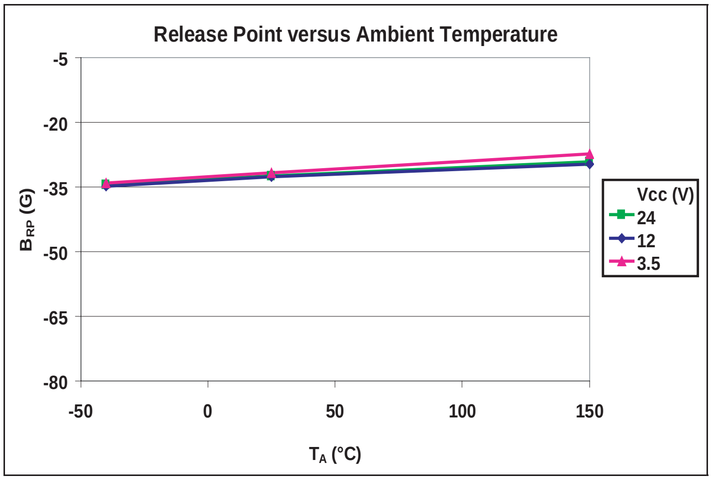


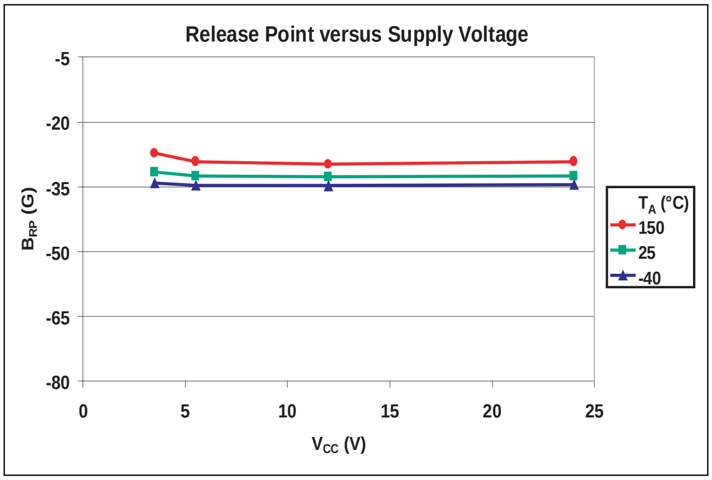


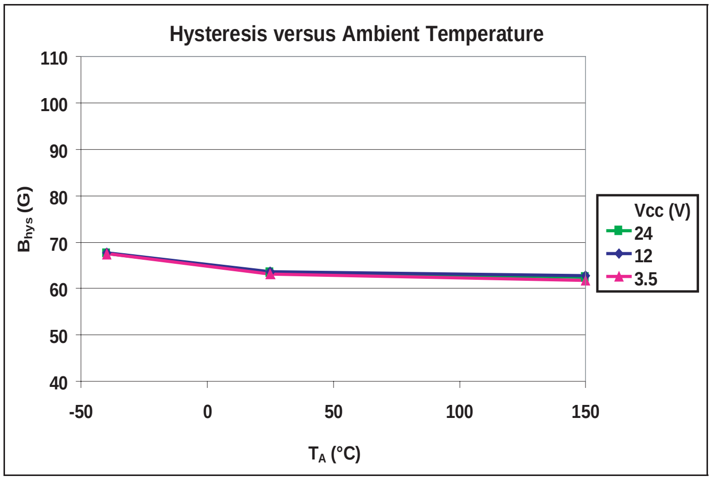


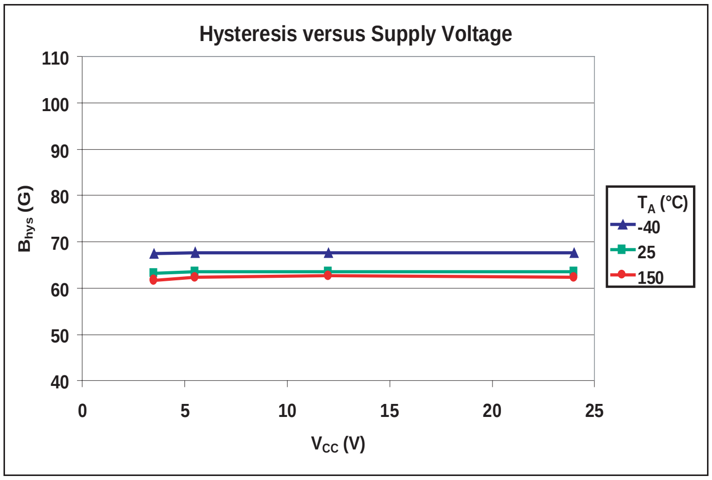

Operate Point versus Ambient Temperature
80
65
50
35
20
5
B_{OP} (G)
-50
0
50
100
150
T_A (°C)
Vcc (V)
24
12
3.5


Operate Point versus Supply Voltage
80
65
50
35
20
5
B_{OP} (G)
0
5
10
15
20
25
V_{CC} (V)
T_A (°C)
-40
25
150


Release Point versus Ambient Temperature
-5
-20
-35
-50
-65
-80
B_{RP} (G)
-50
0
50
100
150
T_A (°C)
Vcc (V)
24
12
3.5


Release Point versus Supply Voltage
-5
-20
-35
-50
-65
-80
B_{RP} (G)
0
5
10
15
20
25
V_{CC} (V)
T_A (°C)
150
25
-40


Hysteresis versus Ambient Temperature
110
100
90
80
70
60
50
40
B_{hys} (G)
-50
0
50
100
150
T_A (°C)
Vcc (V)
24
12
3.5


Hysteresis versus Supply Voltage
110
100
90
80
70
60
50
40
B_{hys} (G)
0
5
10
15
20
25
V_{CC} (V)
T_A (°C)
-40
25
150

Functional Description

OPERATION

The output, I_{CC}, of the A1242 switches to the high current state when a magnetic field perpendicular to the Hall sensor exceeds the operate point threshold, B_{OP}. Note that the device latches, that is, a south pole of sufficient strength towards the branded surface of the device switches the device output to $I_{CC(H)}$. The device retains its output state if the south pole is removed. When the magnetic field is reduced to below the release point threshold, B_{RP}, the device output goes to the low current state. The difference between the magnetic operate and release points is called the hysteresis of the device, B_{HYS}. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

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TYPICAL APPLICATION CIRCUIT

The A1242 should be protected by an external bypass capacitor, C_{BYP}, connected between the supply, V_{CC}, and the ground, GND, of the device. C_{BYP} reduces both external noise and the noise generated by the chopper-stabilization function. As shown in figure 2, a 0.01 μF capacitor is typical.

Installation of C_{BYP} must ensure that the traces that connect it to the A1242 pins are no greater than 5 mm in length.

All high-frequency interferences conducted along the supply lines are passed directly to the load through C_{BYP}, and it serves only to protect the A1242 internal circuitry. As a result, the load ECU (electronic control unit) must have sufficient protection, other than C_{BYP}, installed in parallel with the A1242.

A series resistor on the supply side, R_S (not shown), in combination with C_{BYP}, creates a filter for EMI pulses.

When determining the minimum V_{CC} requirement of the A1242 device, the voltage drops across R_S and the ECU sense resistor, R_{SENSE}, must be taken into consideration. The typical value for R_{SENSE} is approximately 100 Ω.

Extensive applications information on magnets and Hall-effect sensors is available in:

- *Hall-Effect IC Applications Guide,* AN27701,
- *Hall-Effect Devices: Gluing, Potting, Encapsulating, Lead Welding and Lead Forming,* AN27703.1
- *Soldering Methods for Allegro Products – SMD and Through-Hole,* AN26009

All are provided in Allegro Electronic Data Book, AMS-702 and the Allegro Web site: www.allegromicro.com.

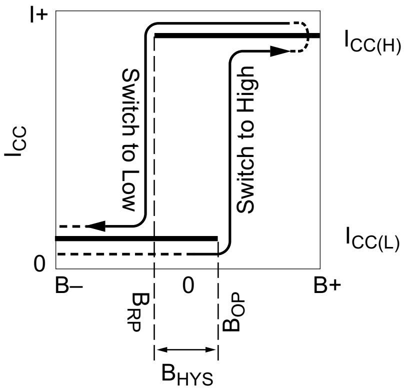


Figure 1. Switching Behavior of the A1242. On the horizontal axis, the B+ direction indicates increasing south polarity magnetic field strength, and the B– direction indicates decreasing south polarity field strength (including the case of increasing north polarity).

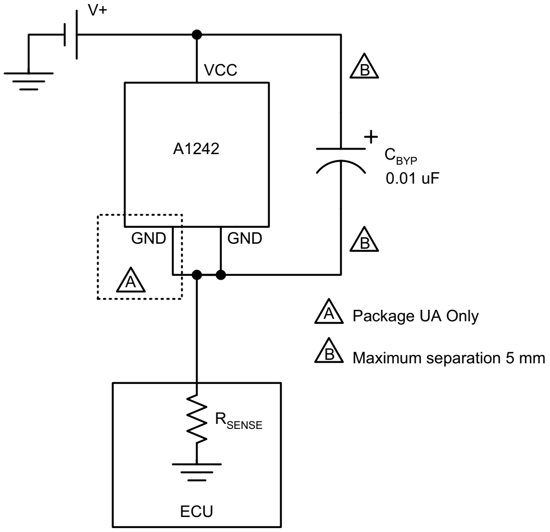


Figure 2. Typical Application Circuit

Chopper Stabilization Technique

When using Hall-effect technology, a limiting factor for switchpoint accuracy is the small signal voltage developed across the Hall element. This voltage is disproportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal while maintaining an accurate, reliable output over the specified operating temperature and voltage ranges.

Chopper stabilization is a unique approach used to minimize Hall offset on the chip. The patented Allegro technique, namely Dynamic Quadrature Offset Cancellation, removes key sources of the output drift induced by thermal and mechanical stresses. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetic field-induced signal in the frequency domain, through modulation. The subsequent demodulation acts as a modulation process for the offset, causing the magnetic field induced signal to recover its original spectrum at baseband, while the dc offset becomes a high-frequency signal. The magnetic sourced signal then can pass through a low-pass filter, while the modulated dc offset is suppressed. This configuration is illustrated in Figure 3.

The chopper stabilization technique uses a 200 kHz high frequency clock. For demodulation process, a sample and hold technique is used, where the sampling is performed at twice the chopper frequency (400 kHz). This high-frequency operation allows a greater sampling rate, which results in higher accuracy and faster signal-processing capability. This approach desensitizes the chip to the effects of thermal and mechanical stresses, and produces devices that have extremely stable quiescent Hall output voltages and precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process, which allows the use of low-offset, low-noise amplifiers in combination with high-density logic integration and sample-and-hold circuits.

The repeatability of magnetic field-induced switching is affected slightly by a chopper technique. However, the Allegro high frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that are more likely to be sensitive to such degradation are those requiring precise sensing of alternating magnetic fields; for example, speed sensing of ring-magnet targets. For such applications,

Allegro recommends its digital sensor families with lower sensitivity to jitter. For more information on those devices, contact your Allegro sales representative.

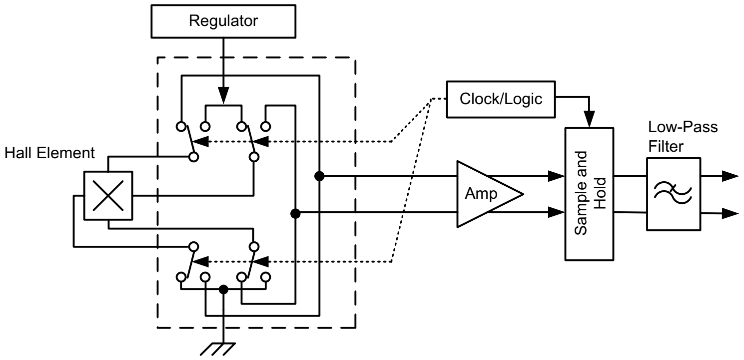


Figure 3. Chopper stabilization circuit (dynamic quadrature offset cancellation)

Power Derating

Power Derating

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \tag{1}$$

$$\Delta T = P_D \times R_{\theta JA} \tag{2}$$

$$T_J = T_A + \Delta T \tag{3}$$

For example, given common conditions such as: $T_A = 25°C$, $V_{CC} = 12$ V, $I_{CC} = 6$ mA, and $R_{\theta JA} = 165$ °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12 \text{ V} \times 6 \text{ mA} = 72 \text{ mW}$$

$$\Delta T = P_D \times R_{\theta JA} = 72 \text{ mW} \times 165 \text{ °C/W} = 12°\text{C}$$

$$T_J = T_A + \Delta T = 25°\text{C} + 12°\text{C} = 37°\text{C}$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at $T_A = 150°C$, package LH, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA} = 228°C/W$, $T_{J(max)} = 165°C$, $V_{CC(max)} = 24$ V, and $I_{CC(max)} = 17$ mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°\text{C} - 150\,°\text{C} = 15\,°\text{C}$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°\text{C} \div 228 \text{ °C/W} = 66 \text{ mW}$$

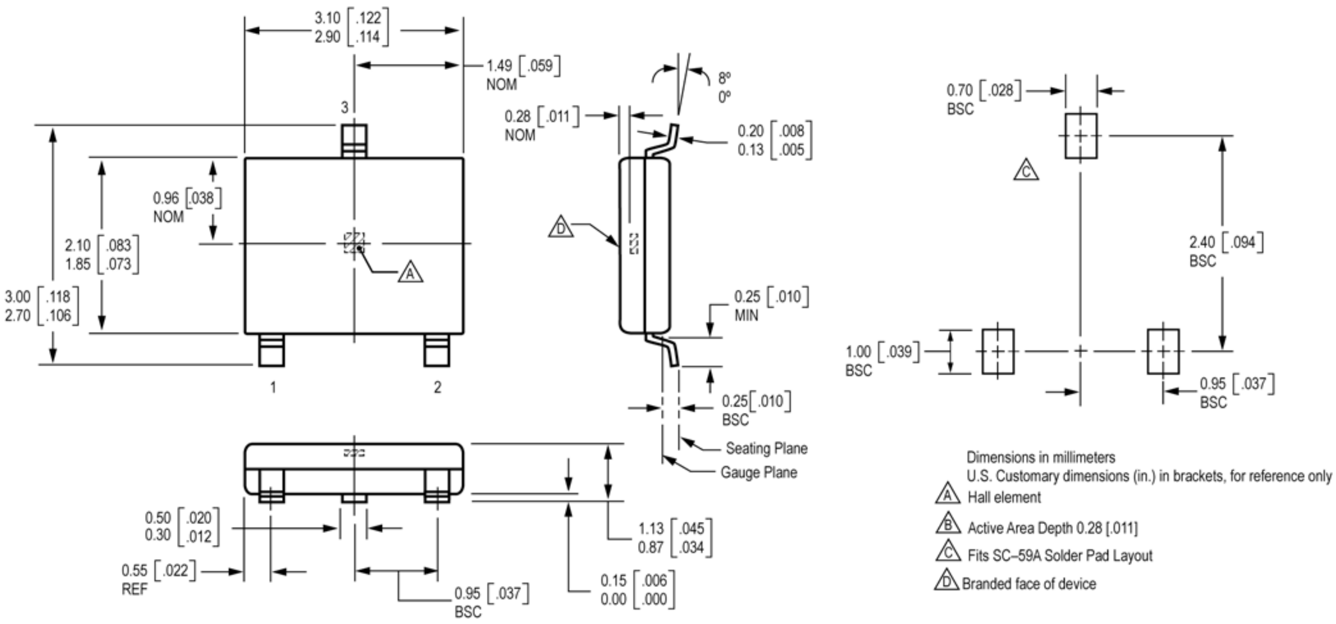
Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 66 \text{ mW} \div 17 \text{ mA} = 3.9 \text{ V}$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages $\leq V_{CC(est)}$.

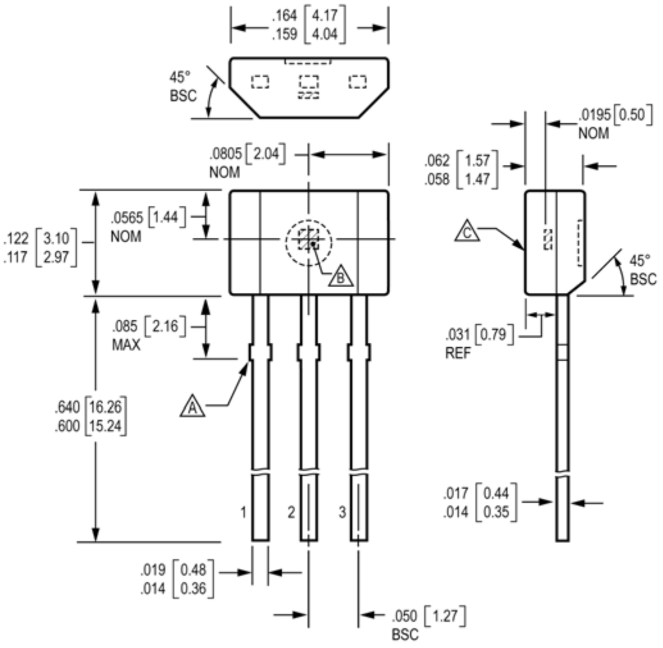
Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

Package LH, 3-Pin (SOT-23W)



Dimensions in millimeters
U.S. Customary dimensions (in.) in brackets, for reference only
A Hall element
B Active Area Depth 0.28 [.011]
C Fits SC–59A Solder Pad Layout
D Branded face of device

Package UA, 3-Pin



Dimensions in inches
Metric dimensions (mm) in brackets, for reference only
A Dambar removal protrusion
B Hall element
C Branded face of device

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.